WHAT IS CLAIMED IS:

1. A serial stream interface for combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:

a slave input interface comprising a slave buffer having a serial input for receiving said slave serial data stream and an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream;

a source selection circuit having a first input channel capable of receiving an N-bit master parallel output from a first master data source and a second input channel coupled to said N-bit slave parallel output; and

a serialization circuit having an input coupled to an output of said source selection circuit capable of receiving a selected one of said N-bit master parallel output and said N-bit slave parallel output and a serial output, wherein said serialization circuit sequentially shifts out each bit of said selected one of said N-bit master parallel output and said N-bit slave parallel output to produce an output serial data stream.

2. The serial stream interface as set forth in Claim 1 wherein each bit in said each N-bit slave data packet stored in said slave buffer becomes available in said N-bit slave parallel output substantially concurrently with storage of said each bit in said slave buffer.

3. The serial stream interface as set forth in Claim 2 wherein said slave buffer is a first-in, first-out (FIFO) device.

4. The serial stream interface as set forth in Claim 3 wherein said slave buffer is a 1xN-bit random access memory (RAM).

5. The serial stream interface as set forth in Claim 1 wherein said slave input interface further comprises a slave control circuit capable of receiving said at least one slave timing signal and generating therefrom at least one storage control signal capable of storing said each of said N-bit slave data packets in said slave buffer.

6. The serial stream interface as set forth in Claim 1 wherein said source selection circuit comprises a first multiplexer having an M-bit output.

7. The serial stream interface as set forth in Claim 6 wherein said serialization circuit comprises a second multiplexer having a first M-bit input channel coupled to said M-bit output of said first multiplexer.

8. The serial stream interface as set forth in Claim 7 wherein said serialization circuit comprises a flip-flop circuit having an M-bit input coupled to an M-bit output of said second multiplexer, wherein said flip-flop latches M-bits of data received from said second multiplexer on an M-bit output of said flip-flop.

9. The serial stream interface as set forth in Claim 8 wherein said second multiplexer further comprises a second M-bit input channel coupled to said M-bit output of said flip-flop.

10. A radio frequency (RF) receiver comprising:

a receiver front-end circuit capable of receiving an incoming RF signal from an antenna and generating an amplified RF output signal;

demodulation circuitry capable of demodulating said amplified RF output signal and generating a plurality of baseband serial data streams;

a serial stream interface capable of receiving said plurality of baseband serial data streams and combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:

a slave input interface comprising a slave buffer having a serial input for receiving said slave serial data stream and an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream;

a source selection circuit having a first input channel capable of receiving an N-bit master parallel output from a first master data source and a second input channel

coupled to said N-bit slave parallel output; and

a serialization circuit having an input coupled to an output of said source selection circuit capable of receiving a selected one of said N-bit master parallel output and said N-bit slave parallel output and a serial output, wherein said serialization circuit sequentially shifts out each bit of said selected one of said N-bit master parallel output and said N-bit slave parallel output to produce an output serial data stream; and

a digital signal processor capable of receiving and processing said output serial data stream.

11. The radio frequency receiver as set forth in Claim 10 wherein each bit in said each N-bit slave data packet stored in said slave buffer becomes available in said N-bit slave parallel output substantially concurrently with storage of said each bit in said slave buffer.

12. The radio frequency receiver as set forth in Claim 11 wherein said slave buffer is a first-in, first-out (FIFO) device.

13. The radio frequency receiver as set forth in Claim 12 wherein said slave buffer is a 1xN-bit random access memory (RAM).

14. The radio frequency receiver as set forth in Claim 10 wherein said slave input interface further comprises a slave control circuit capable of receiving said at least one slave timing signal and generating therefrom at least one storage control signal capable of storing said each of said N-bit slave data packets in said slave buffer.

15. The radio frequency receiver as set forth in Claim 10 wherein said source selection circuit comprises a first multiplexer having an M-bit output.

16. The radio frequency receiver as set forth in Claim 15 wherein said serialization circuit comprises a second multiplexer having a first M-bit input channel coupled to said M-bit output of said first multiplexer.

17. The radio frequency receiver as set forth in Claim 16 wherein said serialization circuit comprises a flip-flop circuit having an M-bit input coupled to an M-bit output of said second multiplexer, wherein said flip-flop latches M-bits of data received from said second multiplexer on an M-bit output of said flip-flop.

18. The radio frequency receiver as set forth in Claim 17 wherein said second multiplexer further comprises a second M-bit input channel coupled to said M-bit output of said flip-flop.

19. A radio frequency (RF) transmitter comprising:

a serial stream interface capable of receiving a plurality of baseband serial data streams from a plurality of baseband data sources and combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:

a slave input interface comprising a slave buffer having a serial input for receiving said slave serial data stream and an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream;

a source selection circuit having a first input channel capable of receiving an N-bit master parallel output from a first master data source and a second input channel coupled to said N-bit slave parallel output; and

a serialization circuit having an input coupled to an output of said source selection circuit capable of receiving a selected one of said N-bit master parallel output and said N-bit slave parallel output and a serial output,

wherein said serialization circuit sequentially shifts out each bit of said selected one of said N-bit master parallel output and said N-bit slave parallel output to produce an output serial data stream;

a digital signal processor capable of receiving and processing said output serial data stream; and

a RF modulation circuit capable of receiving a processed output data stream from said digital signal processor and up-converting said output processed data stream to produce a modulated RF signal.

20. The radio frequency transmitter as set forth in Claim 19 wherein each bit in said each N-bit slave data packet stored in said slave buffer becomes available in said N-bit slave parallel output substantially concurrently with storage of said each bit in said slave buffer.

21. The radio frequency transmitter as set forth in Claim 20 wherein said slave buffer is a first-in, first-out (FIFO) device.

22. The radio frequency transmitter as set forth in Claim 21 wherein said slave buffer is a 1xN-bit random access memory (RAM).

23. The radio frequency transmitter as set forth in Claim 19 wherein said slave input interface further comprises a slave control circuit capable of receiving said at least one slave timing signal and generating therefrom at least one storage control signal capable of storing said each of said N-bit slave data packets in said slave buffer.

24. The radio frequency transmitter as set forth in Claim 19 wherein said source selection circuit comprises a first multiplexer having an M-bit output.

25. The radio frequency transmitter as set forth in Claim 24 wherein said serialization circuit comprises a second multiplexer having a first M-bit input channel coupled to said M-bit output of said first multiplexer.

26. The radio frequency transmitter as set forth in Claim 25 wherein said serialization circuit comprises a flip-flop circuit having an M-bit input coupled to an M-bit output of said second multiplexer, wherein said flip-flop latches M-bits of data received from said second multiplexer on an M-bit output of said flip-flop.

27. The radio frequency transmitter as set forth in Claim 26 wherein said second multiplexer further comprises a second M-bit input channel coupled to said M-bit output of said flip-flop.